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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,143	ASANO ET AL.	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 03/17/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,10-12,25-28* is/are rejected.

7)☒ Claim(s) *6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 25 stand rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al. (6,124,736) as reasons set forth in the office action paper no.9.

With regard to claim 25, figure 3b of Yamashita et al. discloses a first switch comprising two field-effect transistors (T200, T201) each having a source electrode, gate electrode, a drain electrode; and input terminal pad, and a common output terminal pad for the two transistors (T200, T201) of the first switch, the source electrode or the drain electrode of each of the two transistors (T200, T201) of the first switch which are connected to the common output terminal pad (O') of the first switch being connected to the input terminal pads thereof;(IO, I1); a second switch comprising two field-effect transistors (T202, T203) each having a source electrode, gate electrode, a drain electrode; and input terminal pad, and a common output terminal pad for the two transistors (T202, T203) of the second switch, the source electrode or the drain electrode of each of the two transistors (T202, T203) of the second switch which are connected to the common output terminal pad (O) of the second switch being connected to the input terminal pads

thereof;(IO', I1'); two control terminal pads (S,S'), one of the two control terminal pads S' being connected to a gate electrode of one of two transistors of the first switch and a gate electrode of one of the two transistors of the second switch, and another of the two control terminal pads S being connected to a gate electrode of another of the two transistors of the first switch and a gate electrode of another of the two transistors of the second switch.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,7,8,10,11,12,26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (6,124,736) in view of Applicant's prior art (APA) fig.1 as reasons set forth in the office action paper no.9.

With regard to claim 1, Yamashita et al. discloses a first, a second, a third and a fourth field-effect transistors (T200, T201, T202, T203), each of said transistors (T200, T201, T202, T203) having a source electrode, gate electrode, and a drain electrode; a first, a second, a third and a fourth input terminal pad (IO, I1, IO', I1') corresponding to the first, second, third, and fourth transistors (T200, T201, T202, T203), respectively, the source electrode or the drain electrode of each of the four transistors (T200, T201, T202, T203) being connected to the corresponding input terminal pad thereof; a first common output terminal pad (O') connected the

source electrode or the drain electrode of the first transistor (T200) and connected to the source electrode or the drain electrode of the second transistor (T201), the two electrodes of the first and second transistors which are connected to the first common output terminal pad (O') being connected to any of the input terminal pads (IO, I1, IO', I1'); a first control terminal pad (S') connected to the gate electrodes of the first and third transistors (T200, T202); and a second control terminal pad (S) connected to the gate electrodes of the second and fourth transistors (T201, T202). (Note C200, Fig. 3b of Yamashita et al.).

Yamashita et al. does not disclose a semiconductor switching circuit device formed on a substrate, each of transistors having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer of the substrate.

However, APA discloses a semiconductor switching circuit device comprising a transistor formed on a substrate 1 wherein a source electrode 4, a gate electrode 3 and a drain electrode 5 of the transistor are formed on a channel layer 2. (Note fig. 1A of APA).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamashita et al.'s device having a semiconductor switching circuit device formed on a substrate and each of transistors of the switching circuit having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer such as taught by APA because such structure is conventional in the art for forming the field effect transistor device.

With regard to claim 4, Yamashita et al. discloses a first connection connecting the first control terminal pad (S') and the gate electrode of the third transistor (T202), wherein the four transistors (T200, T201, T202, T203) are aligned in a direction forming a row of the first, second, third and fourth transistors (T200, T201, T202, T203) in this order, and wherein the

connection is disposed along the row of the transistors (T200, T201, T202, T203). (Note C200, Fig. 3b of Yamashita et al.).

With regard to claims 2, 11, APA discloses the gate electrode 3 forms a Schottky contact with the channel layer 2 and the source electrode 4 and the drain electrode 5 form an ohmic contact with the channel layer 2. (Note 21-24,page 1, fig 1A of APA).

With regard to claims 3, 12, APA discloses the substrate 1 is made of a compound semiconductor GaAs and each of the transistors (FET1, FET2) is a metal-semiconductor field effect transistor. (Note fig. 1A,1B of APA).

With regard to claim 5, fig. 3(b) of Yamashita et al. disclose all the claimed subject matter except for a resistor is formed between the first control terminal pad and the gate electrode of the third transistor. However, it would have been obvious to one of ordinary skill in the art to form a resistor is formed between the first control terminal pad and the gate electrode of the third transistor because such structure is conventional in the art for preventing the leakage of the high frequency signals through the gate. Note fig. 1B of APA is cited to support for the well know position.

With regard to claim 7, Yamashita et al. discloses a second connection connecting the second control terminal pad (S) and the gate electrode of the second transistor T201, wherein the two connections intersect each other. (Note C200, Fig. 3b of Yamashita et al.).

With regard to claim 8, Yamashita et al. discloses the first, second, third and fourth input terminal pads (IO, I1, IO', I1') are disposed on one side of the device so that each of the pads is placed next to the corresponding transistor and wherein the first and second common output terminal pads (O,O') and the first and second control terminal pads (S,S') are disposed on a side

of the device opposite the side of the device of the four input terminal pads (IO, I1, IO', I1'). (Note C200, Fig. 3b of Yamashita et al.). APA and Yamashita et al. disclose all claimed invention, except the two control terminal pads are placed at both ends of the opposite side of the device and the two common output terminal pads are placed between the two control terminal pads. However, although APA and Yamashita et al. does not teach exact the place of the two control terminal pads the two common output terminal pads as that claimed by Applicant, the place differences are considered obvious design choices and are not patentable unless unobvious or expected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note in re Leshin, 125 USPQ 416.

With regard to claim 10, Yamashita et al. discloses portions of the first and second transistors (T200, T201) are disposed between the first and second input terminal pads (IO, I1,), and wherein portions of the third and fourth transistors (T202, T203) are disposed between the third and fourth input terminal pads (IO', I1'). (Note C200, Fig. 3b of Yamashita et al.)

With regard to claim 26, Yamashita et al. does not disclose each of the first and second switch comprises a single pole double throw switch.

However, APA discloses the switch comprises a single pole double throw switch. (Note line 29, page 1, fig. 1B of APA).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamashita et al.'s device having the switch comprises a single pole double throw switch such as taught by APA because such structure is conventional in the art for forming a high frequencies switching device that can be used in a mobile communication device.

Claims 27,28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (6,124,736).

With regard to claim 27, Yamashita et al. disclose four input terminal pads (IO,IO', I1, I1'); two common output terminal pads (O,O'); no more than two control terminal pads (S,S'). (Note C200, Fig. 3b of Yamashita et al.).

Yamashita et al. disclose all the claimed subject matter except for two single pole double throw switches, each of the switches receiving two high frequency signals through two of the four input terminals and outputting one of the two high frequency signals to one of the two common output terminals in response to a control signal received from one of the control terminal. However, it would have been obvious to one of ordinary skill in the art to form two single pole double throw switches, each of the switches receiving two high frequency signals through two of the four input terminals and outputting one of the two high frequency signals to one of the two common output terminals in response to a control signal received from one of the control terminal because such structure is conventional in the art for forming the two-switching-element switch.

With regard to claim 28, Yamashita et al. disclose all the claimed subject matter except for the four input terminal pads receive two pairs of balanced signals, and the two common output terminal pads output one of the two pairs of the balanced signals selected by signals applied to the two control terminal pads. However, it would have been obvious to one of ordinary skill in the art to form the four input terminal pads receive two pairs of balanced signals, and the two common output terminal pads output one of the two pairs of the balanced signals

selected by signals applied to the two control terminal pads because such structure is conventional in the art for forming the two-switching-element switch.

Allowable Subject Matter

3. Claims 6,9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6,9 are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the resistor comprises a high dopant concentration region as recited in claim 6, the first and second connections are disposed between the row of the four transistors and a row of the control terminal pads and the common output terminal pads as recited in claim 9.

Election/Restrictions

4. This application contains claims 13-24 drawn to an invention nonelected with traverse in Paper No. 8. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Response to Arguments

5. Applicant's arguments filed 3/17/03 have been fully considered but they are not persuasive.

It is argued, at page 3 of the remarks, that "the examiner should have given applicants the option of selecting "species" because the examiner required applicants to elect a single species for prosecution and admitted that claim 1 is a generic claim. In this action, the examiner still maintains that this is an election of species requirement without responding to applicants' arguments" This is an election of species requirement. If applicants traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

It is argued, at page 5 of the remark, that "the lead for the output signal 0' of Yamashita is not the common output terminal pad of claim 25" and "Yamashita thus does not teach or suggest the feature of the common output terminal pad of claim 25". However, C200, Fig. 3b of Yamashita et al. does show the output signal 0' is the common output terminal pad of its circuitry 200.

It is argued, at page 5 of the remark, that "Yamashita does not describe a discrete device that needs terminal pads for external connection. Nowhere in Yamashita is a device having terminals pads described. In the absence of such a description, persons of ordinary skill in the art

would have understood that the logic circuit C200 is a part of larger circuitry and is not a discrete device that requires terminal pads for external connection". However, C200, Fig. 3b of Yamashita et al. does show the output signal 0' is the common output terminal pad of its circuitry 200. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a discrete device that needs terminal pads for external connection) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at page 5 of the remark, that "the lead for the output signal 0' of Yamashita is not connected to the source or drain of each of the transistors" and "neither the source or the drain of each of the transistors T200, T201 of Yamashita is connected to the lead for the output signal 0". However, C200, Fig. 3b of Yamashita et al. does show the source electrode or the drain electrode of each of the two transistors (T200, T201) of the first switch which are indirectly connected to the common output terminal pad (O') of the first switch.

It is argued, at pages 5,6 of the remark, that "Yamashita's logic circuit does not describe any terminal pad as a part of its device structure or the feature that the signal entering the device at the input terminal pads comes out of the device at the common output terminal pad" and "Yamashita's device is not configured to switch high frequency signals, such as CDMA and GPS signals, as is the case with the switching device of claim 27". However, C200, Fig. 3b of Yamashita et al. does show four input terminal pads (IO,IO', I1, I1'); two common output terminal pads (O,O'). It would have been obvious to one of ordinary skill in the art to have the

high frequency signals entering the device at four input terminal pads (IO, IO', I1, I1') and comes out of the device at two common output terminal pads (O,O') because such structure is conventional in the art for forming the two-switching-element switch. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., CDMA and GPS signals) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)

It is argued, at page 6 of the remark, that "claim 1 includes the same feature as claim 25 that the common input terminal pad is connected to the source or the drain of the corresponding transistors. As explained above, Yamashita does not teach or suggest this feature of claim 1. Accordingly, Yamashita and the prior art description of the specification do not teach or suggest the switching device of claim 1 as a whole". However, C200, Fig. 3b of Yamashita et al. does show the source electrode or the drain electrode of each of the two transistors (T200, T201) of the first switch which are indirectly connected to the common output terminal pad (O') of the first switch.

It is argued, at page 6 of the remark, that "without specific suggestion or motivation persons skilled in the art would have not combined the Yamashita's device and the prior art description of the specification to produce the switching device of claim 1" and "the examiner provides no reference to any portion of Yamashita or the specification that provides such a suggestion or motivation". However, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the

rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). It would have been obvious to one of ordinary skill in the art to form the Yamashita et al.'s device having a semiconductor switching circuit device formed on a substrate and each of transistors of the switching circuit having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer such as taught by APA because such structure is conventional in the art for forming the field effect transistor device.

It is argued, at page 7 of the remark, that "Yamashita does not describe these devise structures in the wiring layout level recited in the claims". However, C200, Fig. 3b of Yamashita et al. does show a first connection connecting the first control terminal pad (S') and the gate electrode of the third transistor (T202), wherein the four transistors (T200, T201, T202, T203) are aligned in a direction forming a row of the first, second, third and fourth transistors (T200, T201, T202, T203) in this order, and wherein the connection is disposed along the row of the transistors (T200, T201, T202, T203), and a second connection connecting the second control terminal pad (S) and the gate electrode of the second transistor T201, wherein the two connections intersect each other. Moreover, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the wiring layout level) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns. 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, Applicant's claims 1,25,27 do not distinguish over Yamashita and Applicant's prior art references.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

April 2003

Minh Loan Tran
Primary Examiner